

Listing of the Claims:

1. (Previously Presented) An insulated gate field effect transistor, comprising:
 - a semiconductor body having opposed first and second major surfaces;
 - a source region of a first conductivity type at the first major surface;
 - a body region of a second conductivity type opposite to the first conductivity type under the source region;
 - a drift region of the first conductivity type under the body region;
 - a drain region of the first conductivity type under the drift region, so that the source, body, drift and drain regions extend in that order from the first major surface towards the second major surface; and
 - insulated trenches extending from the first major surface towards the second major surface past the source region and the body region into the drift region, each insulated trench having sidewalls, and including insulator on the sidewalls, at least one conductive gate electrode adjacent to the body region separated from the body region by a gate insulator, and at least one conductive field plate electrode adjacent to the drift region separated from the drift region by a field plate insulator, and a gate-field plate insulator separating the conductive field plate electrode from the conductive gate electrode, the gate-field plate insulator being at least as thick as the field plate insulator, wherein the source regions and the insulated trenches define a pattern of cells across the first major surface; and
 - a doping concentration in the drift region increases from a part of the drift region adjacent to the body region to a part of the drift region adjacent to the drain region the doping concentration in the drift region being at least 50 times greater adjacent to the drain region than adjacent to the body region.
2. (Previously Presented) An insulated gate field effect transistor according to claim 1 in which the conductive gate electrode is of conductive semiconductor doped to be the second conductivity type.

3. (Previously Presented) An insulated gate field effect transistor according to claim 1 wherein the conductive gate electrode has side pieces spaced apart adjacent to the sidewalls on either side of the insulated trench and a top piece spanning a gap between the side pieces.
4. (Previously Presented) An insulated gate field effect transistor according to claim 1 wherein a breakdown voltage of the insulated gate field effect transistor is less than or equal to 30V.
5. (Previously Presented) An insulated gate field effect transistor according to claim 1 wherein the pattern of cells defined by the source regions and the insulated trenches arranged across the first major surface is a pattern in which cells repeat in more than one direction across the first major surface to form a three-dimensional cell structure.
6. (Original) An insulated gate field effect transistor according to claim 5 wherein the cells are arranged in a hexagonal pattern.
7. (Previously Presented) An insulated gate field effect transistor according to claim 1 further comprising an additional trench filled with conductive material extending through the source region to the body region to connect a source contact to the source region and the body region.
8. (Previously Presented) An insulated gate field effect transistor according to claim 7 further comprising
a doped contact region of the second conductivity type in the body region in contact with the conductive material in the additional trench, a doping concentration in the doped contact region being higher than a doping concentration in the rest of the body region.

9. (Previously Presented) An insulated gate field effect transistor according to claim 1 wherein a thickness of the insulator adjacent to the conductive field plate electrode is greater than a thickness of the insulator adjacent to the conductive gate electrode.
10. (Previously Presented) An insulated gate field effect transistor according to claim 1 wherein the pattern of cells has a cell pitch not greater than 1 micron.
11. (Previously Presented) An insulated gate field effect transistor according to claim 1 wherein the first conductivity type is n-type, the second conductivity type is p-type and the conductive gate electrode is of p-type doped polysilicon.
12. (Previously Presented) An insulated gate field effect transistor according to claim 1 wherein the field plate insulator has a thickness between 0.6 to 1 microns and the gate insulator has a thickness between 0.2 to 0.5 microns.
13. (Previously Presented) An insulated gate field effect transistor according to claim 1 wherein the conductive field plate electrode is connected to the source region.
14. (Previously Presented) An insulated gate field effect transistor according to claim 1 further comprising
a field plate terminal connected to the conductive field plate electrode for controlling a field plate voltage independently.
15. (Previously Presented) An insulated gate field effect transistor, comprising:
a semiconductor body having opposed first and second major surfaces;
a source region of a first conductivity type at the first major surface;
a body region of a second conductivity type opposite to the first conductivity type under the source region;
a drift region of the first conductivity type under the body region;

a drain region of the first conductivity type under the drift region, so that the source, body, drift and drain regions extend in that order from the first major surface towards the second major surface; and

insulated trenches extending from the first major surface towards the second major surface past the source region and the body region into the drift region, each insulated trench having sidewalls, and including insulator on the sidewalls, at least one conductive gate electrode adjacent to the body region separated from the body region by a gate insulator, and at least one conductive field plate electrode adjacent to the drift region separated from the drift region by a field plate insulator, and a gate-field plate insulator separating the conductive field plate electrode from the conductive gate electrode, the gate-field plate insulator being thicker than the field plate insulator,

wherein the source regions and the insulated trenches define a pattern of cells across the first major surface; and

wherein the drift region has a graded doping concentration that increases from a part of the drift region adjacent to the body region to a part of the drift region adjacent to the drain region, the doping concentration in the part of the drift region adjacent to the drain region being at least 50 times greater than the doping concentration in the part of the drift region adjacent to the body region.

16. (Previously Presented) An insulated gate field effect transistor according to claim 15, wherein the doping concentration in the part of the drift region adjacent to the drain region is at least 200 times greater than the doping concentration in the part of the drift region adjacent to the body region.

17. (Previously Presented) An insulated gate field effect transistor according to claim 15, wherein the doping concentration in the part of the drift region adjacent to the drain region is at least 100 times greater than the doping concentration in the part of the drift region adjacent to the body region.

18. (Previously Presented) An insulated gate field effect transistor according to claim 15, further comprising a source contact and an additional trench filled with conductive material, the additional trench extending through the source region to the body region, the conductive material in the additional trench connecting the source contact to the source region and to the body region.

19. (Previously Presented) An insulated gate field effect transistor, comprising:
a semiconductor body having opposed first and second major surfaces;
a source region at the first major surface, a body region under the source region, a drift region under the body region, and a drain region under the drift region, the drift region having a doping concentration that increases from a part of the drift region adjacent to the body region to a part of the drift region adjacent to the drain region, the doping concentration in the drift region being at least 50 times greater adjacent to the drain region than adjacent to the body region; and
a plurality of insulated trenches extending from the first major surface into the drift region, each of the insulated trenches including
at least one conductive gate electrode adjacent to the body region and separated from the body region by a gate insulator,
at least one conductive field plate electrode adjacent to the drift region and separated from the drift region by a field plate insulator, and
a gate-field plate insulator separating the conductive field plate electrode from the conductive gate electrode, the gate-field plate insulator being at least as thick as the field plate insulator,
wherein the source regions and the insulated trenches define a pattern of cells across the first major surface.

20. (Previously Presented) An insulated gate field effect transistor according to claim 19, wherein the conductive gate electrode in each of the insulated trenches includes
two vertical side pieces spaced apart from each other and adjacent to sidewalls on either side of the insulated trench, and
a horizontal top piece spanning a gap between and connecting the two side pieces.

21. (Previously Presented) An insulated gate field effect transistor according to claim 15, wherein the drift region has a steeply graded doping concentration that is defined by the ratio of the doping concentration of the part of the drift region adjacent to the drain_region to the doping concentration of the part of the drift region adjacent to the body region and wherein the ratio is greater than at least one of: 50, 100 or 200.